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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/344,847	06/28/1999	GAJINDER SINGH PANESAR	S1022/8249	9525

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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/344,847	Applicant(s) PANESAR, GAJINDER SINGH	
	Examiner Kandasamy Thangavelu	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June, 1999 & December 9, 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 1-9 of the application are pending.

Information Disclosure Statement

2. Acknowledgment is made of the information disclosure statements filed on June 28, 1999 together with copies of the patents and papers. The patents and papers have been considered in reviewing the claims.

Drawings

3. The drawings sent on August 10, 1999 are accepted by the examiner with the following objection.

In Fig. 7, "STATE PERIPUCAL" is incorrect. Appropriate correction is required.

Specification

4. The disclosure is objected to because of the following informalities:

Page 2, Lines 31-32, "by allocating specific elements ... to predefine sectors" is incorrect.

Page 7, Line 2, "that is externally of the ASP" is incorrect.

Page 8, Line 24, "the data structure defined in the input file 24" is incorrect.

Page 9, Line 26, "The test functions take the form define the attributes of the CPU" is incorrect.

Page 11, Line 25, "whether entity read or writable" is incorrect.

Page 12, Lines 16-17, "Its contents are checked and any areas are reported" is incorrect.

Appropriate corrections are required.

5. The description portion of this application contains a computer program listing consisting of more than ten (10) pages. In accordance with 37 CFR 1.96(c), a computer program listing printout of more than ten pages must be submitted as a "microfiche appendix" conforming to the standards set forth in 37 CFR 1.96(c)(2) and must be appropriately referenced in the specification (see 37 CFR 1.77(a)(6)). Accordingly, applicant is required to cancel the computer program listing appearing in the specification on pages 17-31, file a "microfiche appendix" in compliance with 37 CFR 1.96(c) and insert an appropriate reference to the newly added "microfiche appendix" at the beginning of the specification.

Claim Objections

6. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

7. Claim 5 is objected to because of the following informalities:

Claim 5, Lines 10-11, "allocating specific elements ... to predefine sectors" is incorrect.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

8. Claim 9 is rejected under 35 U.S.C. 101, as reciting nonfunctional descriptive material. See MPEP Section 2106(II)(A) and 2106(IV)(B)(1).

8.1 Regarding Claim 9, the claim is directed at a register definition file stored on a computer readable medium and comprising a plurality of register definition tables and each table including the word location of the register. Merely claiming nonfunctional descriptive material stored in a computer readable medium does not make the invention eligible for patenting. The claimed invention as a whole must produce a "useful, concrete and tangible" result to have a practical application.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

10. The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Aleksic et al. (AL)** (U.S. Patent 5,995,736) in view of **Shimabukuro et al. (SH)** (U.S. Patent 5,557,774).

11.1 **AL** teaches method and system for automatically modeling registers for integrated circuit design. Specifically, as per Claim 1, **AL** teaches a method of operating a computer system to design an application specific processor (ASP) (Col 1, Lines 6-9) comprising:

entering the input file into the computer system and operating a modelling tool loaded on the computer system to generate from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table (Col 1, Lines 58-61; Col 2, Lines 29-39 and Col 3, Lines 53-66; Fig 6A) ; and

using the register definition file to create in silicon the registers of the ASP (Col 5, Lines 19-29; Fig. 3, item 62).

AL does not expressly teach that the method comprises defining a set of peripherals for the ASP which are responsive to stimuli and which communicate with a processor. **SH** teaches that the method comprises defining a set of peripherals for the ASP which are responsive to

stimuli and which communicate with a processor, ***in order to model and simulate the behavior of an actual computer system with peripherals.*** (Col 4, Lines 7-13). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **AL** with the method of **SH** that included defining a set of peripherals for the ASP which are responsive to stimuli and which communicate with a processor, as that would facilitate ***modeling and simulating the behavior of an actual computer system with peripherals***.

AL does not expressly teach that the method comprises generating for each peripheral an input file which defines the functional attributes of that peripheral in a high level language with an input data structure. **SH** teaches that the method comprises generating for each peripheral an input file which defines the functional attributes of that peripheral in a high level language with an input data structure, ***in order to model and simulate the behavior of an actual computer system with peripherals.*** (Col 4, Lines 15-24; Col 3, Lines 30-35 and Col 7, Lines 13-21). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **AL** with the method of **SH** that included defining a set of peripherals for the ASP which are responsive to stimuli and which communicate with a processor, as that would facilitate ***modeling and simulating the behavior of an actual computer system with peripherals***.

11.2 As per Claim 2, **AL** and **SH** teach the method of Claim 1. **AL** also teaches that each input file comprises a data structure which defines for each of a set of registers the name of an element in the register, the bit length of the element, the functional status of the element and the function of the element. (Col 3, Lines 61-66 and Figure 7, Item 49).

11.3 As per Claim 3, **AL** and **SH** teach the method of Claim 1. **AL** also teaches that each register definition table includes at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element. (Col 3, Lines 61-66 and Figure 7, Item 49).

11.4 As per Claim 4, **AL** and **SH** teach the method of Claim 1. **AL** does not expressly teach that the register definition table includes the word location of the register within a memory map for access during simulation of the ASP. **SH** teaches that the register definition table includes the word location of the register within a memory map for access during simulation of the ASP, ***in order to generate the test environment programs automatically.*** (Fig 3, Item 302; Fig. 4, Items 303 and 403). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **AL** with the method of **SH** that included the register definition table having the word location of the register within a memory map for access during simulation of the ASP, as that would facilitate ***generating the test environment programs automatically***.

11.5 As per Claim 5, **AL** teaches a computer system which comprises a processor and a memory, the memory holding a program representing a modelling tool for use in designing an application specific processor (ASP) (Col 1, Lines 6-9; Col 3, Line 53 to Col 4, Line 3; Fig. 4);

the computer system comprises an input means for receiving a plurality of input files (Fig 2 and Fig 3);

the processor being operable to execute the program representing the modelling tool to generate from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table (Col 1, Lines 58-61; Col 2, Lines 29-39 and Col 3, Lines 53-66; Fig 6A); and

the computer system comprises an output means for outputting the register definition file in a manner which is usable to create in silicon the registers of the ASP (Col 5, Lines 19-29; Fig. 3, item 62).

AL does not expressly teach each input file defining the functional attributes of a peripheral for the ASP in a high level language within an input data structure. **SH** teaches each input file defining the functional attributes of a peripheral for the ASP in a high level language within an input data structure, ***in order to model and simulate the behavior of an actual computer system with peripherals.*** (Col 4, Lines 15-24; Col 3, Lines 30-35 and Col 7, Lines 13-21). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer system of **AL** with the computer system of **SH** that included defining the functional attributes of a peripheral for the ASP in a high level language within an input data structure, as that would facilitate ***modeling and simulating the behavior of an actual computer system with peripherals***.

11.6 As per Claim 6, **AL** and **SH** teach the computer system of Claim 5. **AL** also teaches that the input means comprises means for receiving a physical recording device holding the input file for each peripheral. (Fig. 4). Official notice is taken that the Computer having the processor

and memory shown in Figure 4 has the input means comprising means for receiving a physical recording device holding the input file for each peripheral.

11.7 As per Claim 7, **AL** and **SH** teach the computer system of Claim 5. **AL** also teaches that the output means comprises means for loading the register definition file onto a physical recording device. (Fig. 4). Official notice is taken that the Computer having the processor and memory shown in Figure 4 has the output means comprising means for loading the register definition file onto a physical recording device.

11.8 As per Claim 8, **AL** teaches a computer program product stored on a computer readable medium and comprising software code portions operable when executed by a computer to read an input file which defines an input date structure (Col 1, Lines 6-9; Col 3, Line 53 to Col 4, Line 3; Fig. 4); and

to generate from that input file a register definition file, the software code portions including a code portion for allocating specific elements of the input data structure to predefined sectors of a register definition table for each of a plurality of registers (Col 1, Lines 58-61; Col 2, Lines 29-39 and Col 3, Lines 53-66; Fig 6A).

AL does not expressly teach a computer program product comprising software code to read an input file which defines in an input date structure the functional attributes of a peripheral for an application specific processor in a high level language. **SH** teaches a computer program product comprising software code to read an input file which defines in an input date structure the functional attributes of a peripheral for an application specific processor in a high level

language, ***in order to model and simulate the behavior of an actual computer system with peripherals.*** (Col 4, Lines 15-24; Col 3, Lines 30-35 and Col 7, Lines 13-21). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer program product of **AL** with the computer program product of **SH** that included software code for reading an input file which defines in an input date structure the functional attributes of a peripheral for an application specific processor in a high level language, as that would facilitate ***modeling and simulating the behavior of an actual computer system with peripherals***.

11.9 As per Claim 9, **AL** teaches a register definition file stored on a computer readable medium and comprising a plurality of register definition tables (Col 3, Lines –56; Fig. 7, Item 49); and

each table including at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element (Col 3, Lines –56; Fig. 7, Item 49).

AL does not expressly teach each table including the word location of the register within a memory map for access during simulation of an ASP implementing the registers. **SH** teaches each table including the word location of the register within a memory map for access during simulation of an ASP implementing the registers, ***in order to generate the test environment programs automatically.*** (Col 4, Lines 15-24; Col 3, Lines 30-35 and Col 7, Lines 13-21). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the register definition file of **AL** with the register definition file of **SH** that included each

table having the word location of the register within a memory map for access during simulation of an ASP implementing the registers, as that would facilitate ***generating the test environment programs automatically***.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to downloading firmware files and compressed firmware files.

1. Lin et al., "Coverification system and method", U.S. Patent 6,389,379, May, 2002.

2. Schiefele, "Reconfigurable expert rule processing system", U.S. Patent 6,314,416, November, 2001.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7329.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
June 28, 2002

SAMUEL BRODA, ESQ.
PATENT EXAMINER